1. A semiconductor memory device having at least one memory cell, said at least one memory cell including a switching element and a capacitive element connected in series with said switching element, wherein said capacitive element has a ferroelectric body, and the polarization axis of said ferroelectric body is substantially parallel to a predetermined direction of an electric field across said capacitive element, and wherein said capacitive element is provided above said switching element.

2. A semiconductor memory device having at least one memory cell, said at least one memory cell including a switching element, said switching element having a first electrode, a second electrode and a gate electrode, and a capacitive element connected to said first electrode in series with said switching element, wherein said capacitive element has a ferroelectric body, and the polarization axis of said ferroelectric body is substantially parallel to a predetermined direction of an electric field across said capacitive element, and wherein said ferroelectric body is provided above said first electrode.

3. A semiconductor memory device according to claim 1 or 2, wherein said ferroelectric body is comprised of a plurality of ferroelectric crystals and each of said crystals has a surface parallel to said polarization axis.

4. A semiconductor device comprising:

a substrate,

a connector attached to the substrate, and

a plurality of memories provided on the substrate,

wherein each of the memories includes a semiconductor memory device according to claim 1 or 2.

5. A semiconductor device according to claim 4, wherein the semiconductor device is a semiconductor disk.

6. A semiconductor device according to claim 4, wherein the semiconductor device is a semiconductor memory card.

7. A microprocessor including a cache memory having the semiconductor memory device according to claim 1 or claim 2.

8. A computer system comprising:

a microprocessor,

a memory, and

a system bus to which said microprocessor and said memory are connected,

wherein said microprocessor includes a cache memory having the semiconductor memory device according to claim 1 or claim 2.

9. A computer system comprising:

a microprocessor,

a memory, and

a system bus to which said microprocessor and said memory are connected,

wherein said memory includes the semiconductor memory device according to claim 1 or claim 2.

10. A computer system comprising:

a microprocessor,

a memory connected to said microprocessor, and

an I/O control connected to said microprocessor,

wherein said microprocessor includes a cache memory having the semiconductor memory device according to claim 1 or claim 2.

11. A computer system comprising:

a microprocessor,

a memory connected to said microprocessor, and

an I/C control connected to said microprocessor,

wherein said memory includes the semiconductor memory device according to claim 1 or claim 2.

12. An engine control apparatus comprising:

an I/O control,

a microprocessor connected to said I/O control, and

a memory connected to said I/O control,

wherein an engine is controlled via said I/O control by said microprocessor and said memory, and

wherein said microprocessor includes a cache memory having the semiconductor memory device according to claim 1 or claim 2.

13. An engine control apparatus comprising:

an I/O control,

a microprocessor connected to said I/O control, and

a memory connected to said I/O control,

wherein an engine is controlled via said I/O control by said microprocessor and said memory, and

wherein said memory includes the semiconductor memory device according to claim 1 or claim 2.

14. An engine control apparatus according to claim 12, wherein said engine is installed in any one of a vehicle, an air craft, an artificial satellite, a space station and a rocket.

15. An engine control apparatus according to claim 13, wherein said engine is installed in any one of a vehicle, an air craft, an artificial satellite, a space station and a rocket.

16. A method of controlling an engine which is coupled to a microprocessor, and I/O control and a memory, wherein said memory includes a switching element and a capacitive element connected in series with said switching element, wherein said capacitive element has a ferroelectric body, and the polarization axis of said ferroelectric body is substantially parallel to a predetermined direction of an electric field across said capacitive element, and wherein said capacitive element is provided above said switching element, said method comprising:

controlling said engine by said microprocessor and said memory through said I/O control by detecting a change in polarization of the ferroelectric capacitor when a voltage is applied which is not sufficient to cause a change of state of the ferroelectric capacitor.

17. A method according to claim 16, wherein a plurality of said ferroelectric capacitors are connected to said switching element, said method further comprising:

writing different data into different ones of said ferroelectric capacitors.